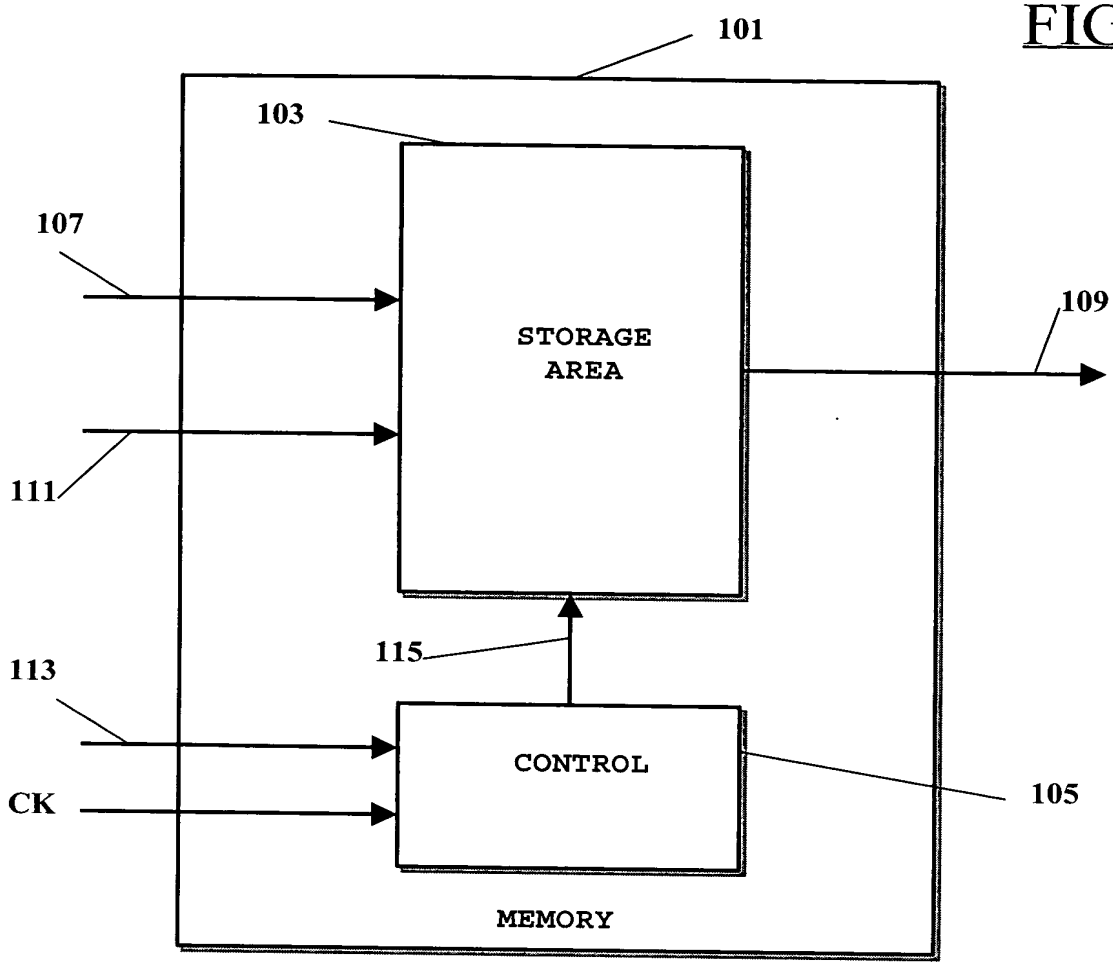
FIG.1


101
103
107
STORAGE AREA
109
111
115
113
CONTROL
105
CK
MEMORY

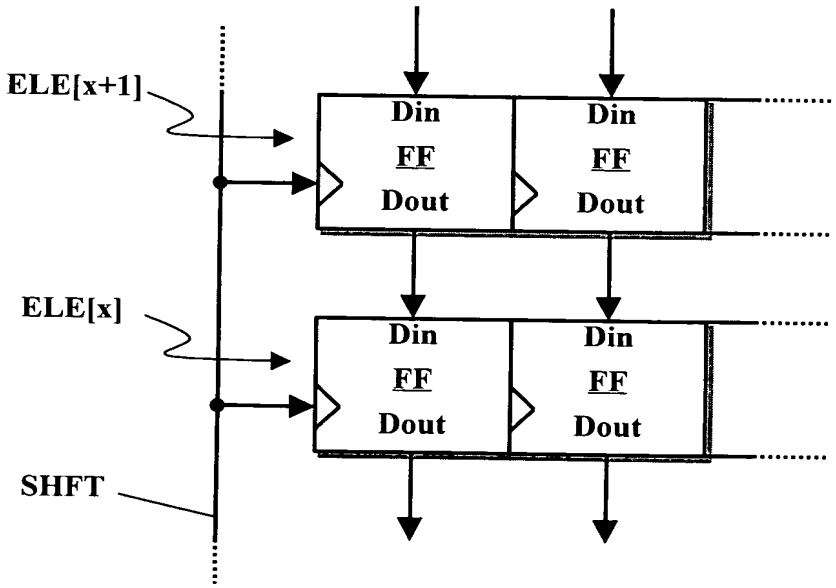

ELE[x+1]
Din
FF
Dout
Din
FF
Dout
ELE[x]
Din
FF
Dout
Din
FF
Dout
SHFT

FIG.2B

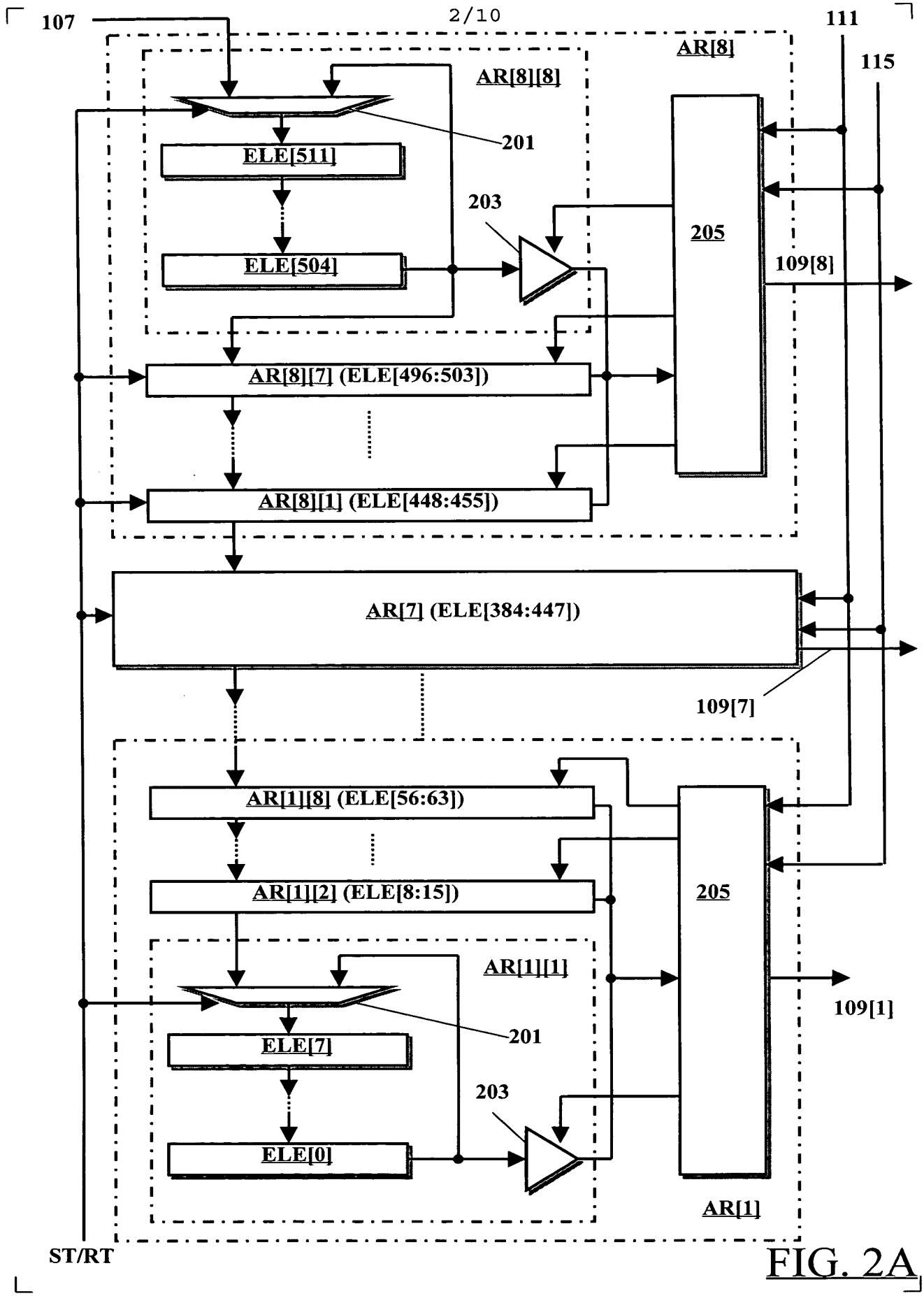

107
111
115
AR[8]
AR[8][8]
201
ELE[511]
ELE[504]
203
205
109[8]
AR[8][7] (ELE[496:503])
AR[8][1] (ELE[448:455])
AR[7] (ELE[384:447])
109[7]
AR[1][8] (ELE[56:63])
AR[1][2] (ELE[8:15])
205
AR[1][1]
201
ELE[7]
ELE[0]
203
109[1]
AR[1]
ST/RT

FIG. 2A

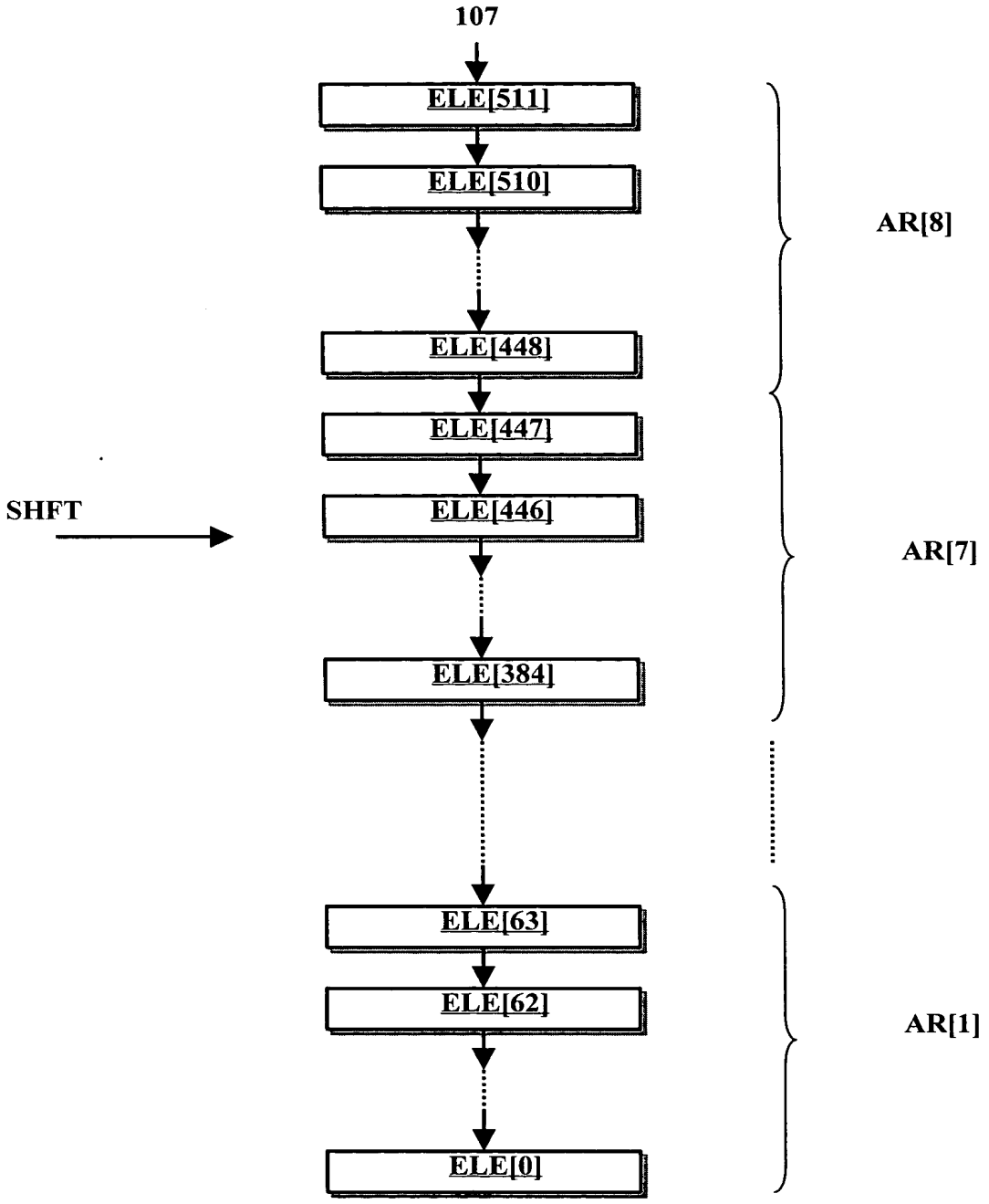

107
ELE[511]
ELE[510]
AR[8]
ELE[448]
ELE[447]
SHFT
ELE[446]
AR[7]
ELE[384]
ELE[63]
ELE[62]
AR[1]
ELE[0]

FIG. 3

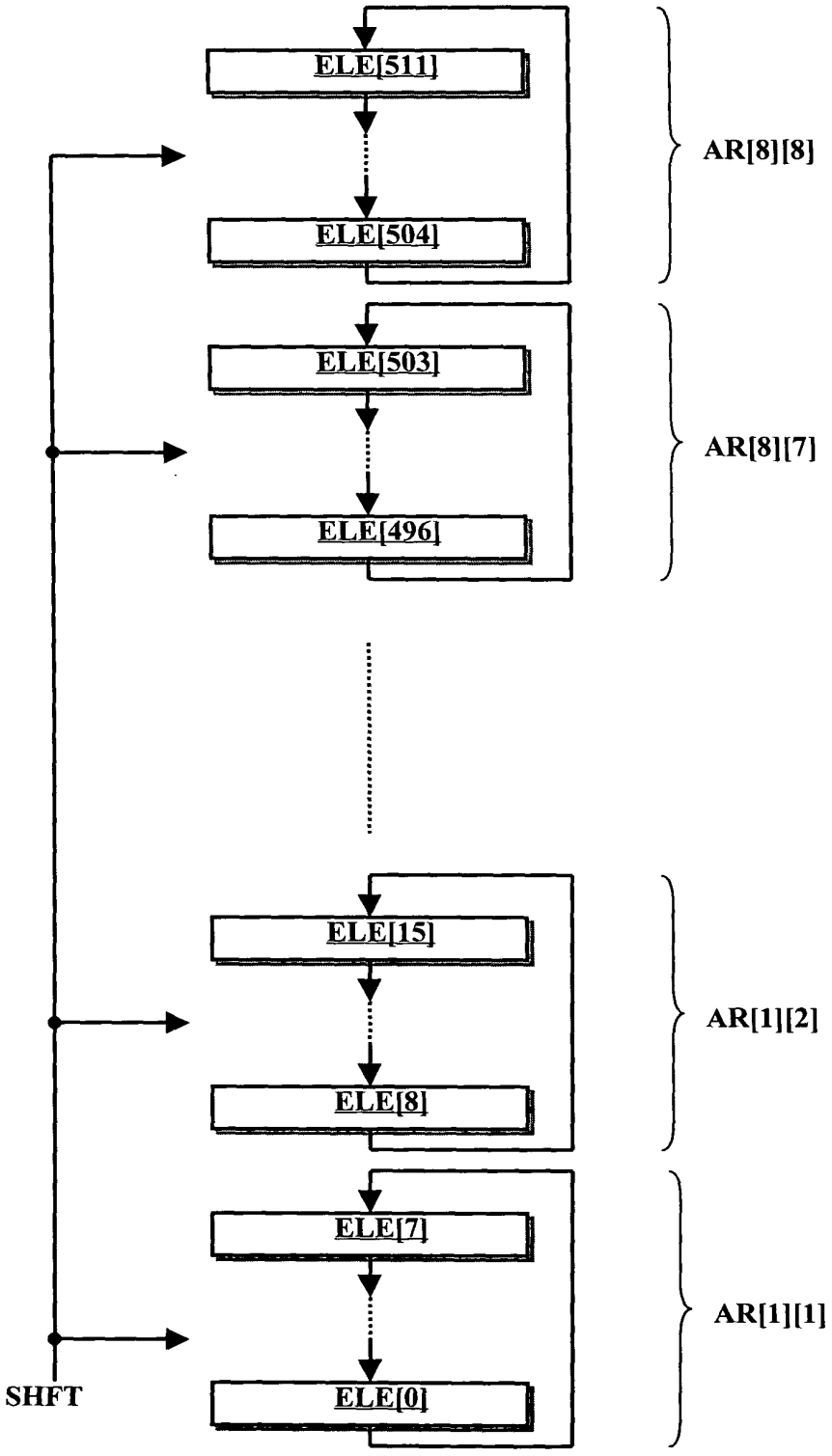

ELE[511]
ELE[504]
AR[8][8]
ELE[503]
ELE[496]
AR[8][7]
ELE[15]
ELE[8]
AR[1][2]
ELE[7]
ELE[0]
AR[1][1]
SHFT

FIG. 4

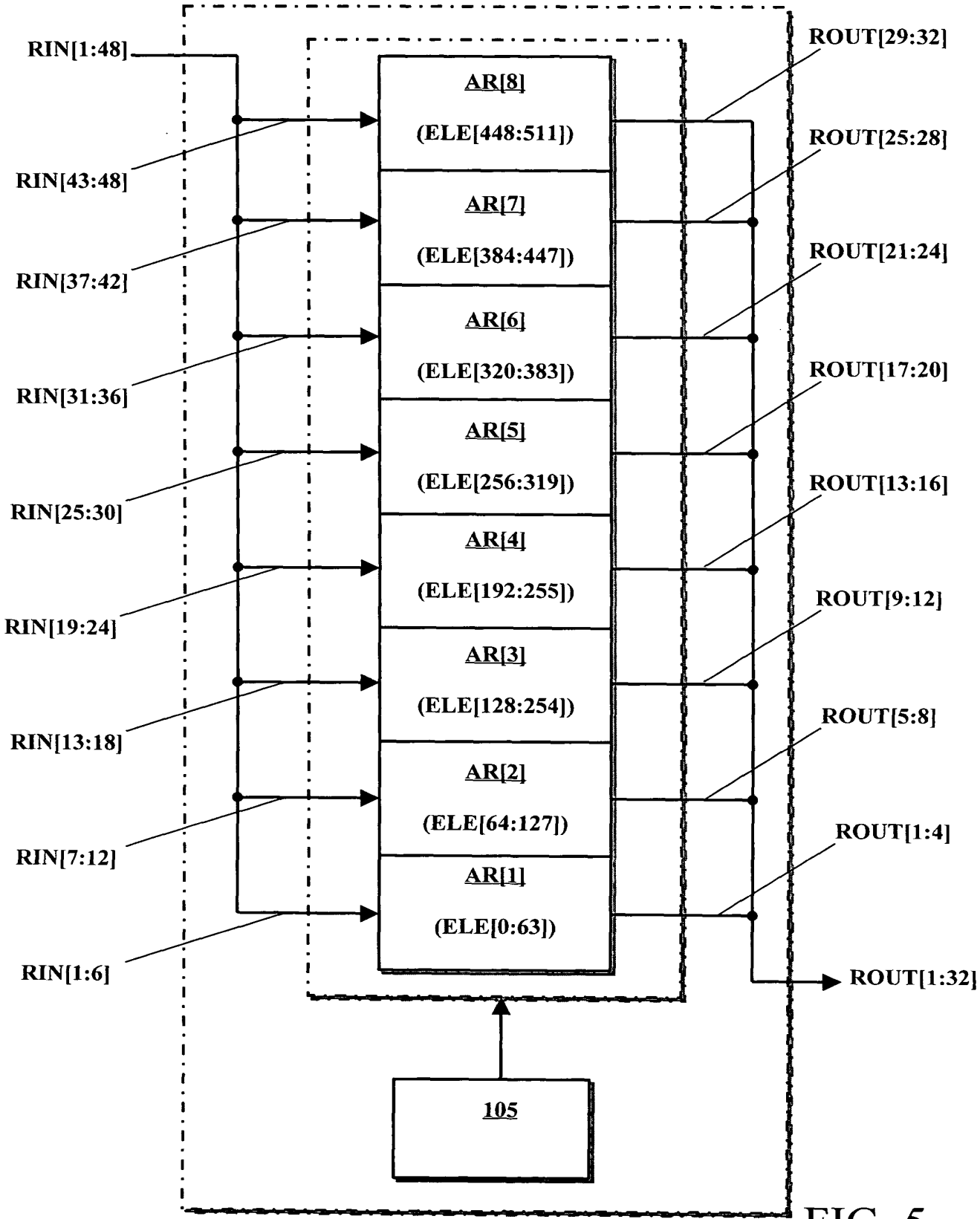

RIN[1:48]
RIN[43:48]
RIN[37:42]
RIN[31:36]
RIN[25:30]
RIN[19:24]
RIN[13:18]
RIN[7:12]
RIN[1:6]
AR[8]
(ELE[448:511])
AR[7]
(ELE[384:447])
AR[6]
(ELE[320:383])
AR[5]
(ELE[256:319])
AR[4]
(ELE[192:255])
AR[3]
(ELE[128:254])
AR[2]
(ELE[64:127])
AR[1]
(ELE[0:63])
105
ROUT[29:32]
ROUT[25:28]
ROUT[21:24]
ROUT[17:20]
ROUT[13:16]
ROUT[9:12]
ROUT[5:8]
ROUT[1:4]
ROUT[1:32]

FIG. 5

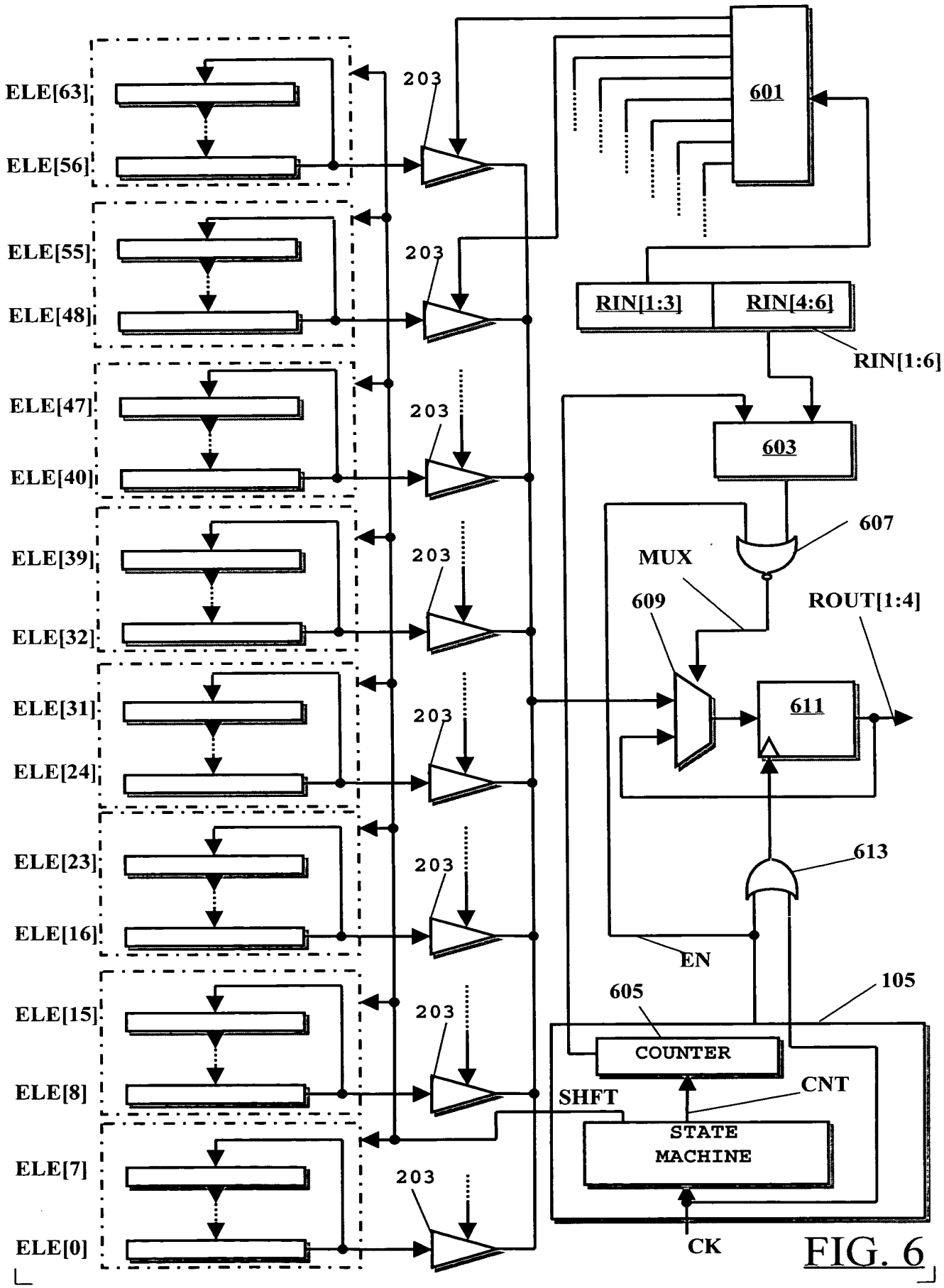

ELE[63]
ELE[56]
ELE[55]
ELE[48]
ELE[47]
ELE[40]
ELE[39]
ELE[32]
ELE[31]
ELE[24]
ELE[23]
ELE[16]
ELE[15]
ELE[8]
ELE[7]
ELE[0]
203
601
RIN[1:3]
RIN[4:6]
RIN[1:6]
603
607
MUX
609
ROUT[1:4]
611
613
EN
105
605
COUNTER
CNT
SHFT
STATE MACHINE
CK

FIG. 6

FIG. 7A

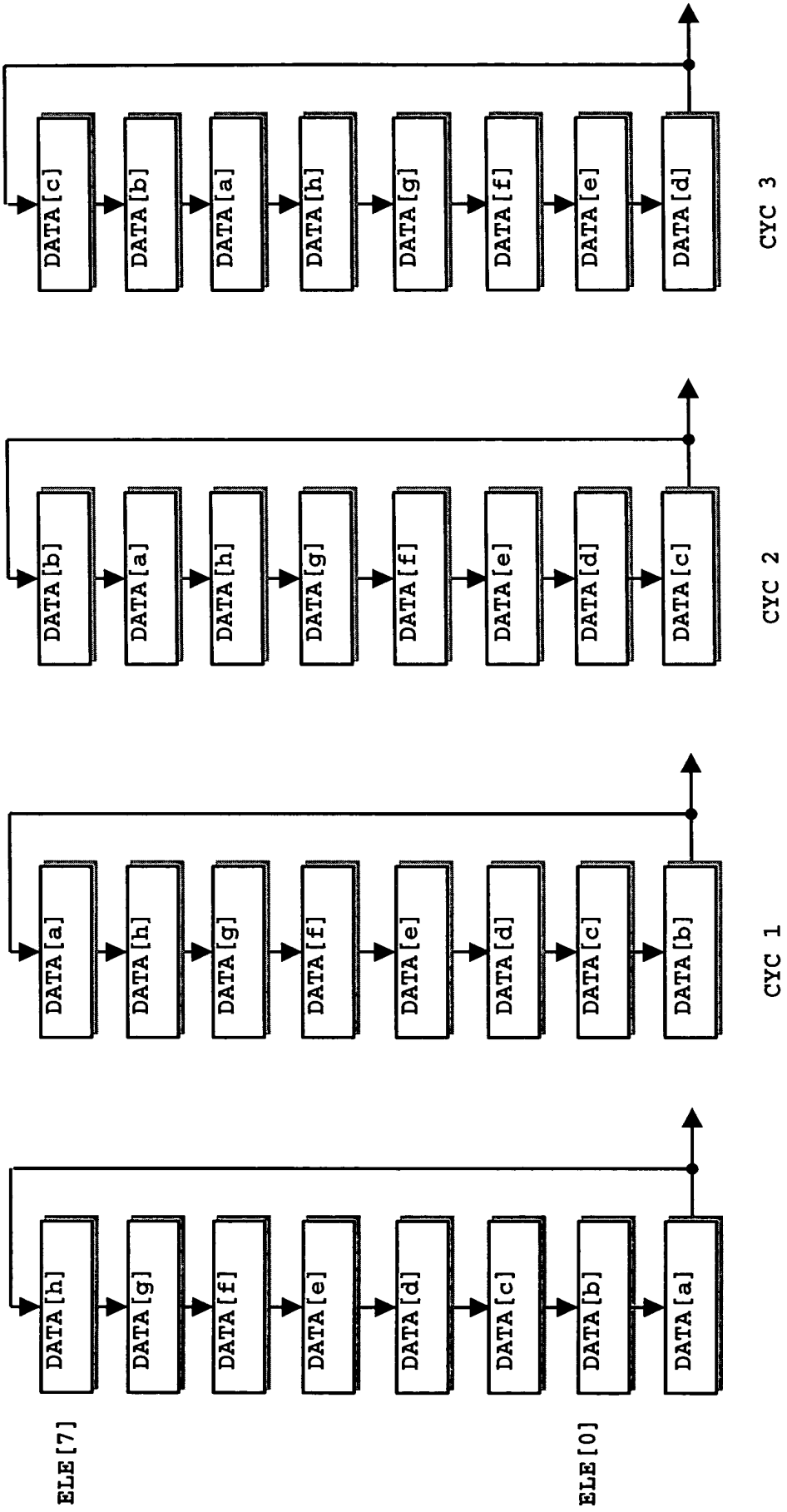

ELE[7]
ELE[0]
DATA[h]
DATA[g]
DATA[f]
DATA[e]
DATA[d]
DATA[c]
DATA[b]
DATA[a]
CYC 1
DATA[a]
DATA[h]
DATA[g]
DATA[f]
DATA[e]
DATA[d]
DATA[c]
DATA[b]
CYC 2
DATA[b]
DATA[a]
DATA[h]
DATA[g]
DATA[f]
DATA[e]
DATA[d]
DATA[c]
CYC 3
DATA[c]
DATA[b]
DATA[a]
DATA[h]
DATA[g]
DATA[f]
DATA[e]
DATA[d]

FIG. 7B

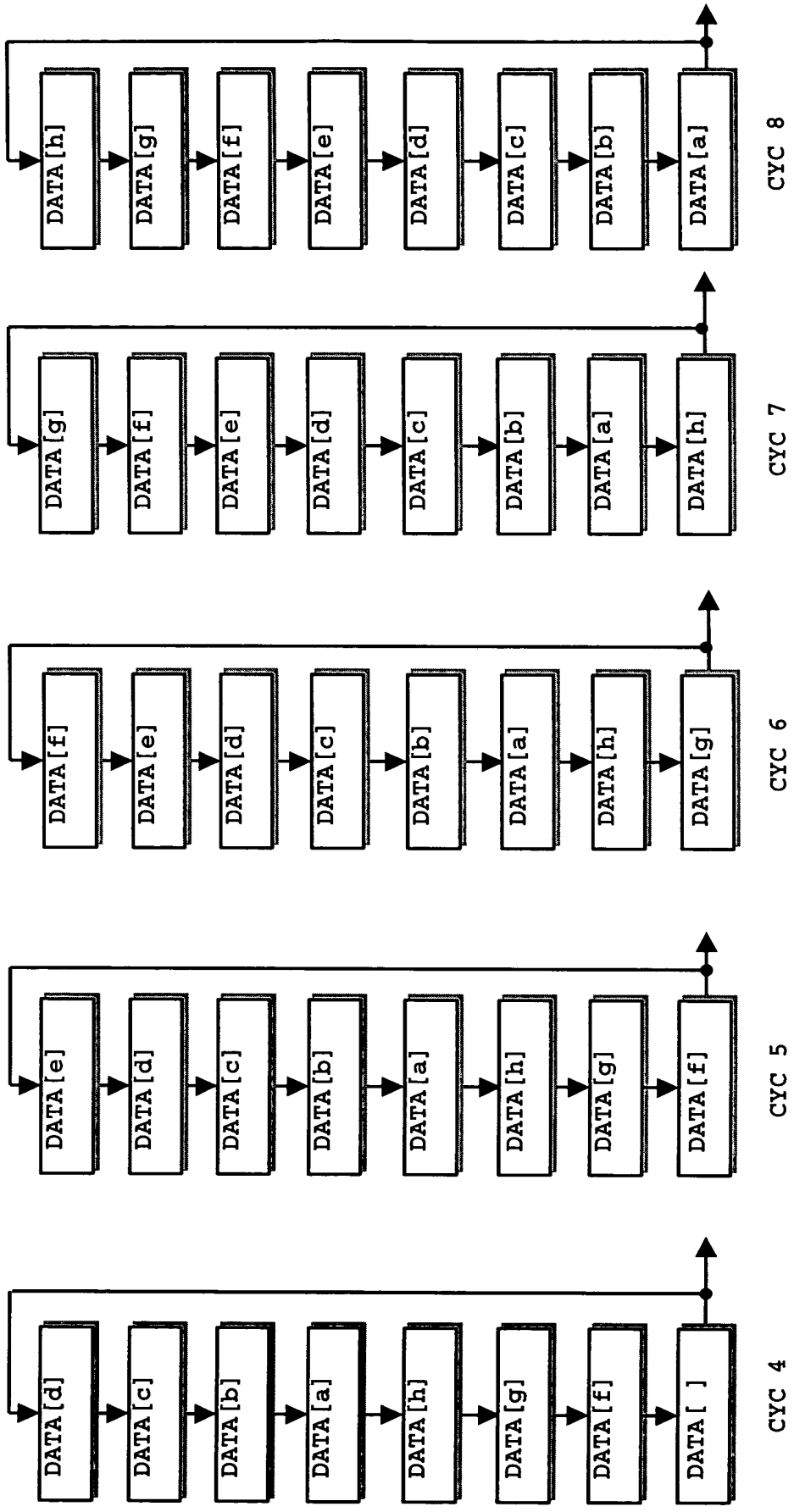

DATA[d]
DATA[c]
DATA[b]
DATA[a]
DATA[h]
DATA[g]
DATA[f]
DATA[ ]
CYC 4
DATA[e]
DATA[d]
DATA[c]
DATA[b]
DATA[a]
DATA[h]
DATA[g]
DATA[f]
CYC 5
DATA[f]
DATA[e]
DATA[d]
DATA[c]
DATA[b]
DATA[a]
DATA[h]
DATA[g]
CYC 6
DATA[g]
DATA[f]
DATA[e]
DATA[d]
DATA[c]
DATA[b]
DATA[a]
DATA[h]
CYC 7
DATA[h]
DATA[g]
DATA[f]
DATA[e]
DATA[d]
DATA[c]
DATA[b]
DATA[a]
CYC 8

FIG.8

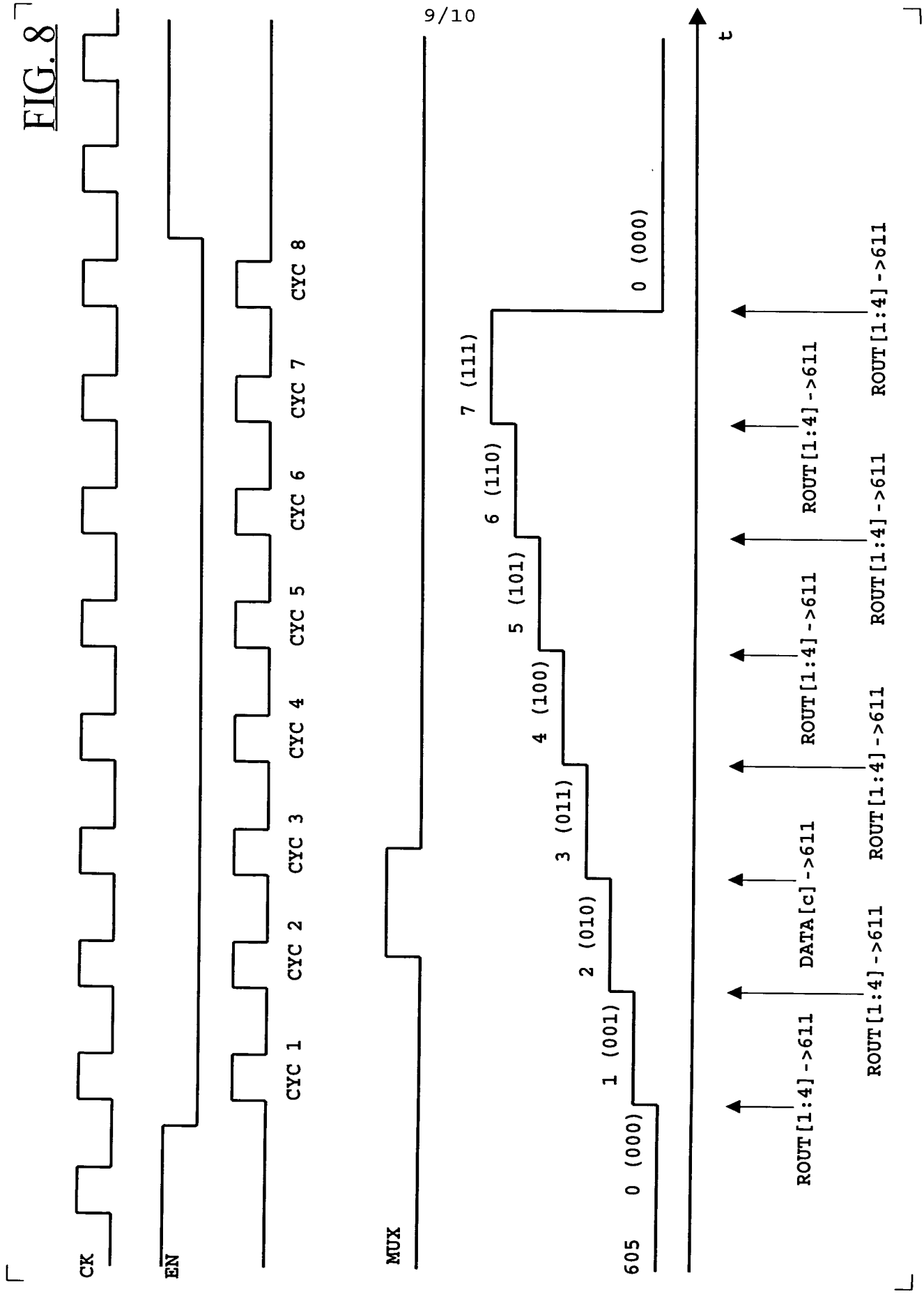
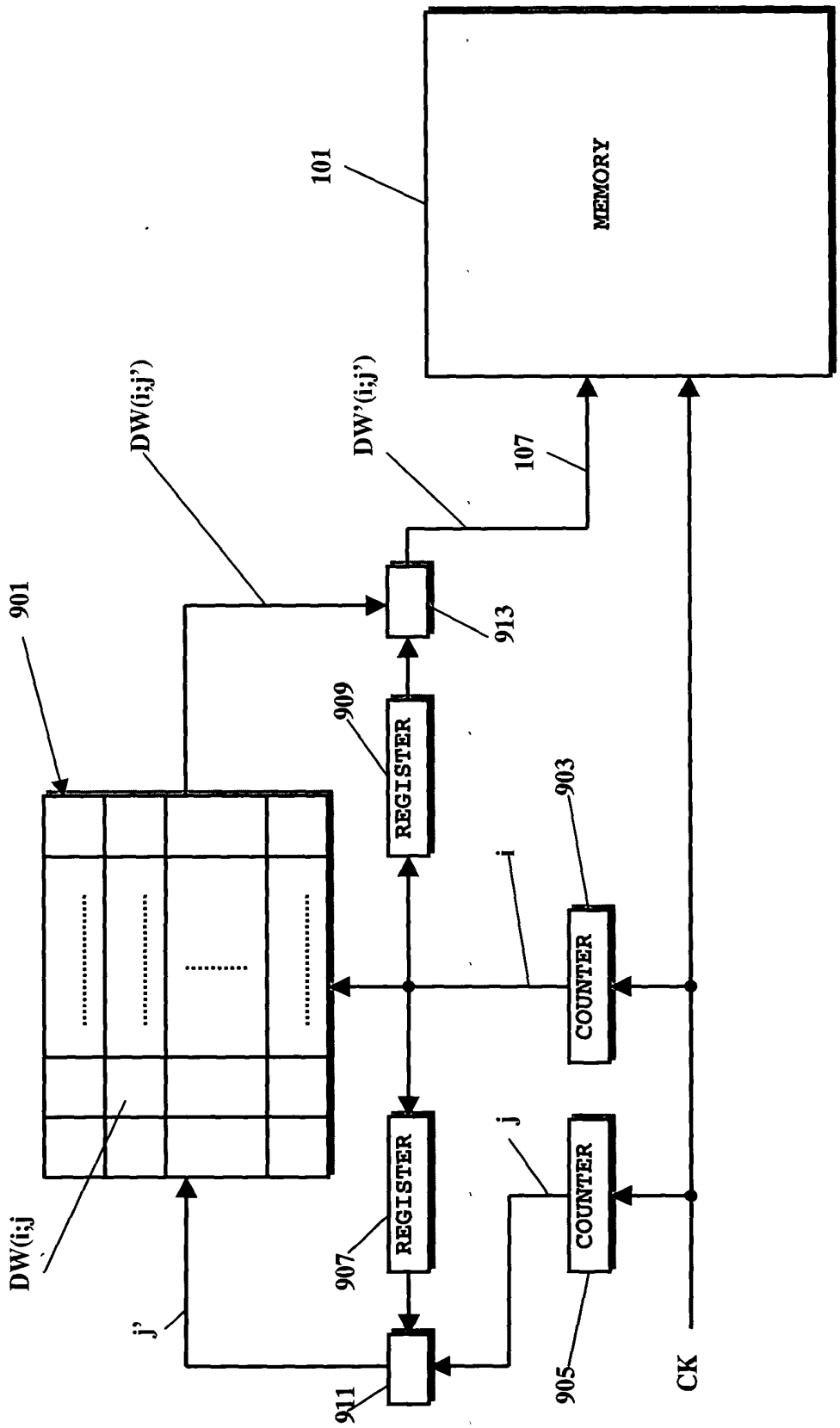

CK
EN
MUX
CYC 1
CYC 2
CYC 3
CYC 4
CYC 5
CYC 6
CYC 7
CYC 8
605
0 (000)
1 (001)
2 (010)
3 (011)
4 (100)
5 (101)
6 (110)
7 (111)
0 (000)
t
ROUT[1:4]->611
DATA[c]->611
ROUT[1:4]->611
ROUT[1:4]->611
ROUT[1:4]->611
ROUT[1:4]->611
ROUT[1:4]->611
ROUT[1:4]->611

FIG. 9


101
MEMORY
DW(i;j')
DW'(i;j')
107
901
913
909
REGISTER
903
i
COUNTER
DW(i;j
907
REGISTER
j
COUNTER
j'
911
905
CK